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Chung

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(54) **OTP MEMORIES FUNCTIONING AS AN MTP MEMORY**

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(71) Applicant: **Shine C. Chung**, San Jose, CA (US)

(72) Inventor: **Shine C. Chung**, San Jose, CA (US)

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Primary Examiner — Alexander Sofocleous

Assistant Examiner — Muhammad Islam

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See application file for complete search history.

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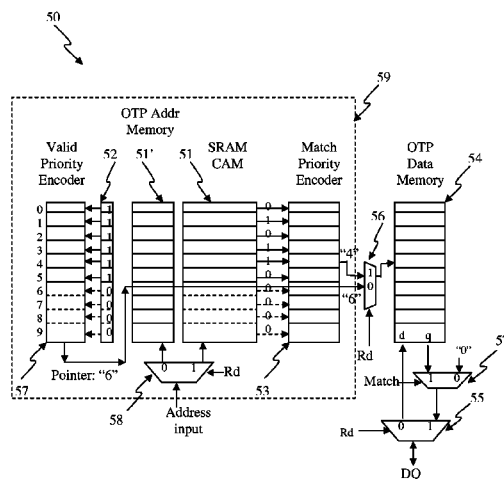
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ABSTRACT

Techniques, systems and circuitry for using One-Time Programmable (OTP) memories to function as a Multiple-Time Programmable (MTP) memory. The OTP-for-MTP memory can include at least one OTP data memory to store data, and at least one OTP CAM to store addresses and to search input address through valid entries of the OTP CAM to find a latest entry of the matched valid addresses. The OTP-for-MTP memory can also include a valid-bit memory to find a next available entry of the OTP data memory and OTP CAM. When programming the OTP-for-MTP memory, address and data can be both programmed into the next available entry of the OTP CAM and the OTP data memory, respectively. When reading the OTP-for-MTP memory, the input address can be used to compare with valid entries of the addresses stored in the OTP CAM so that the latest entry of the matched valid addresses can be output.

21 Claims, 11 Drawing Sheets



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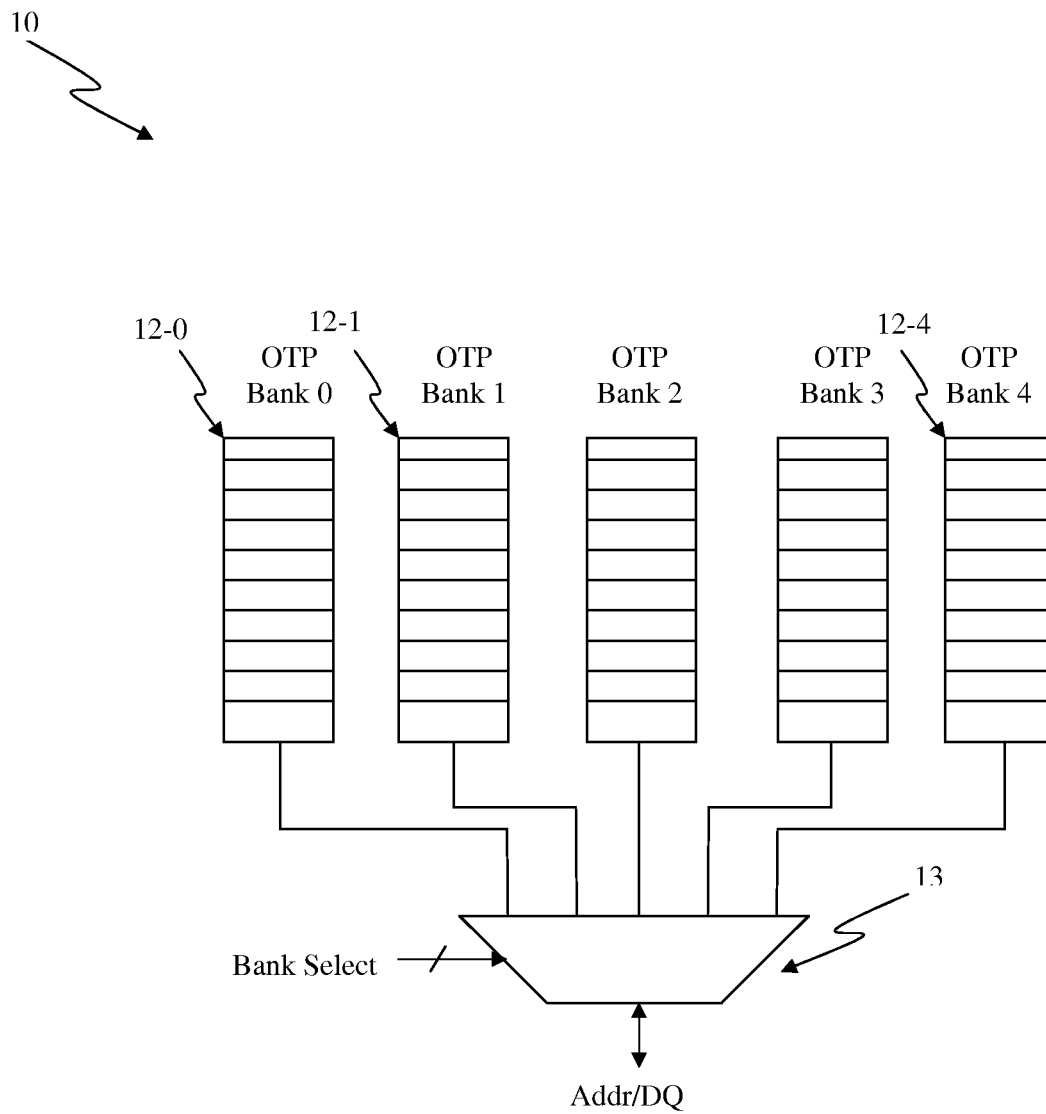
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**FIG. 1 (prior art)**

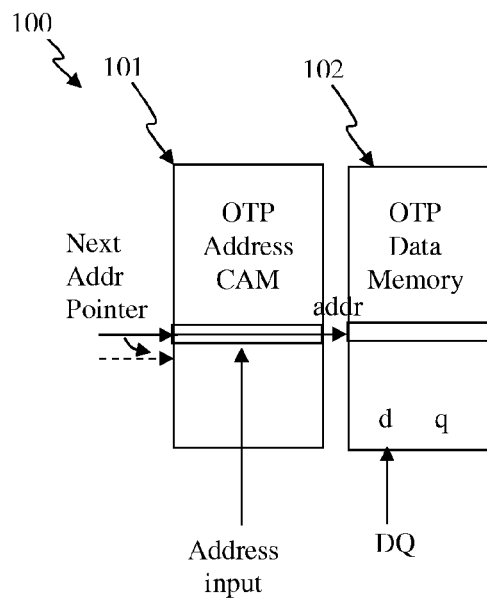


FIG. 2(a)

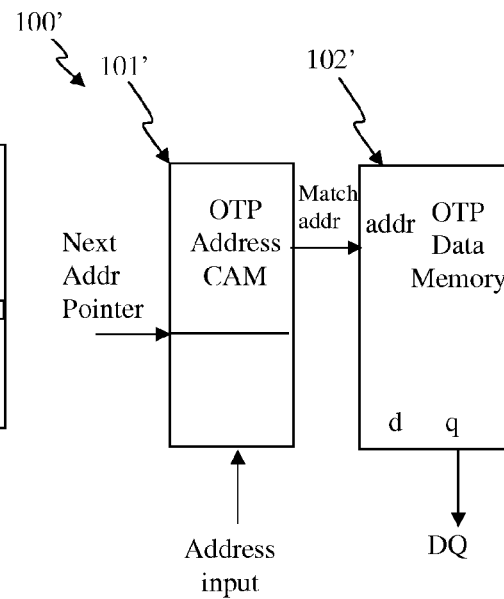


FIG. 2(b)

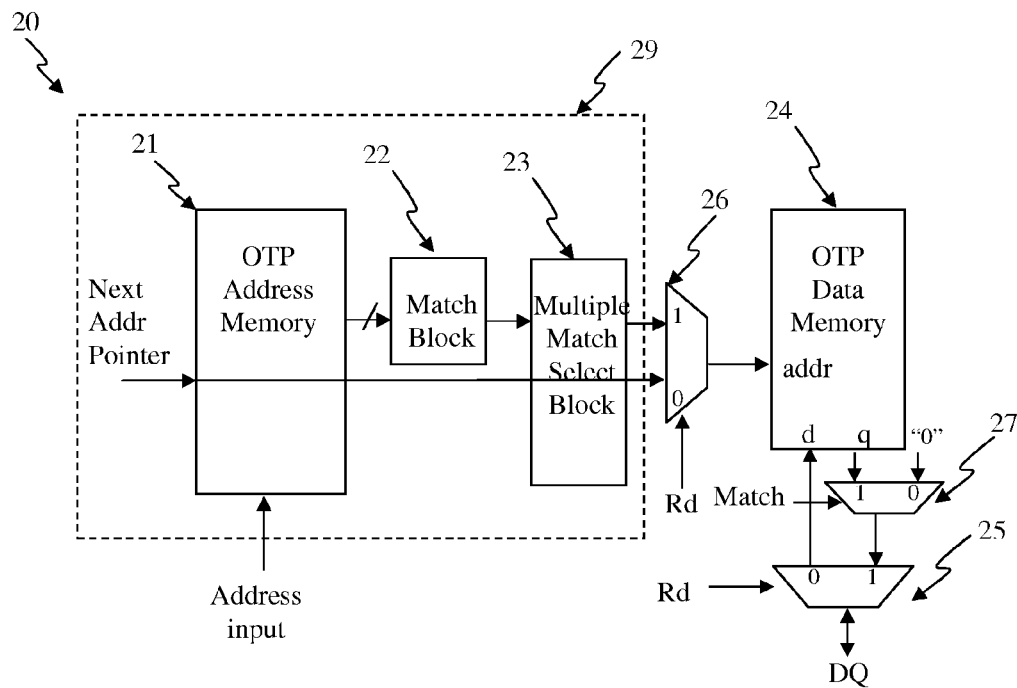


FIG. 2(c)

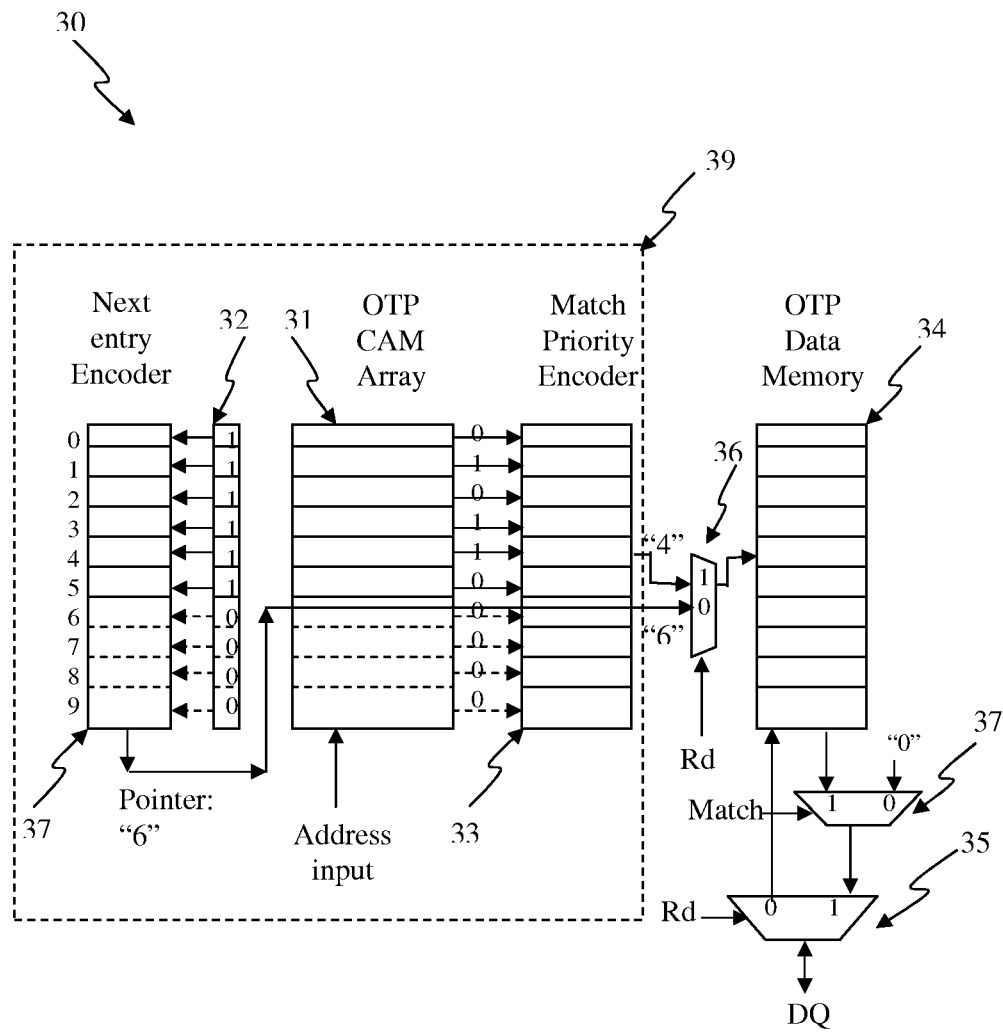


FIG. 3(a)

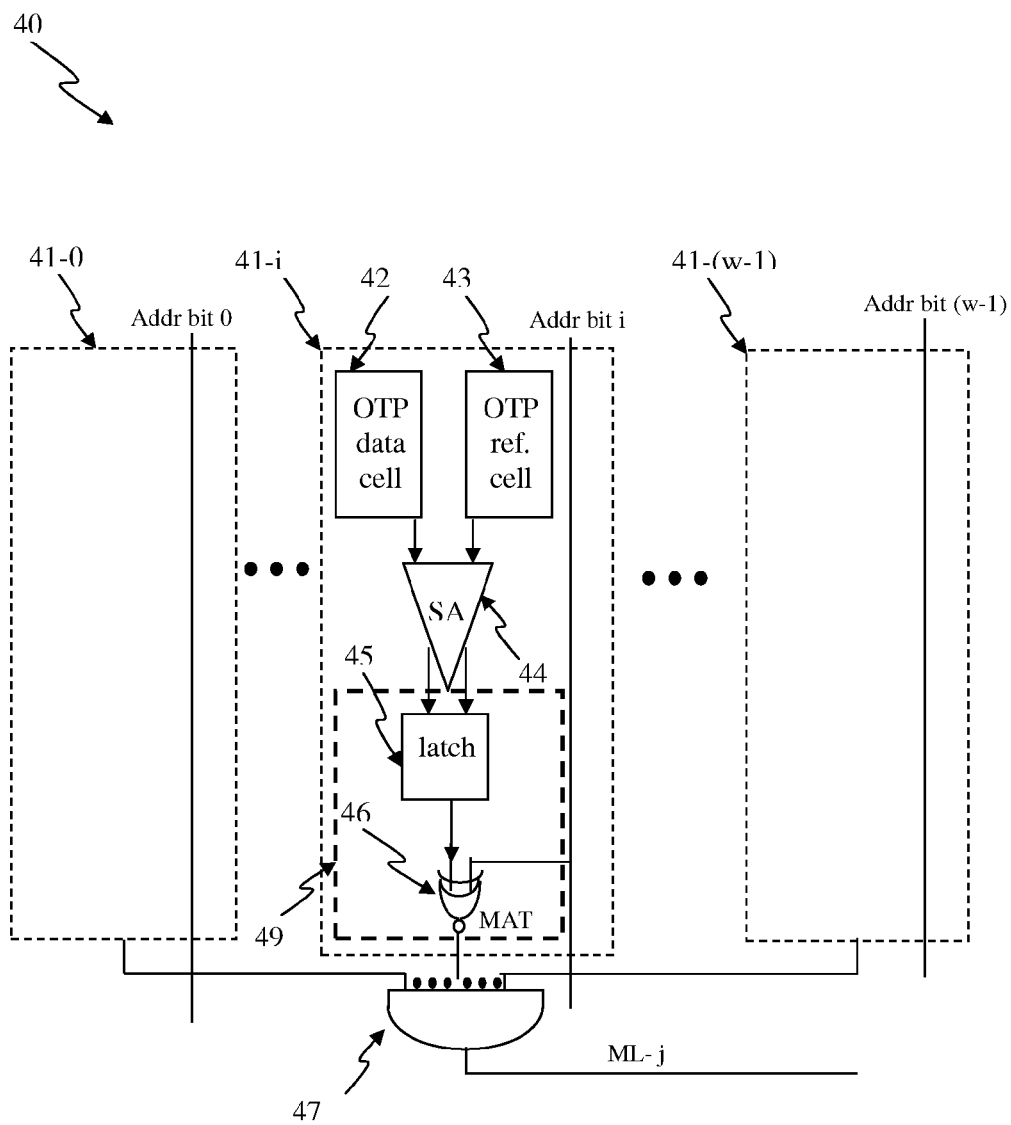


FIG. 3(b)

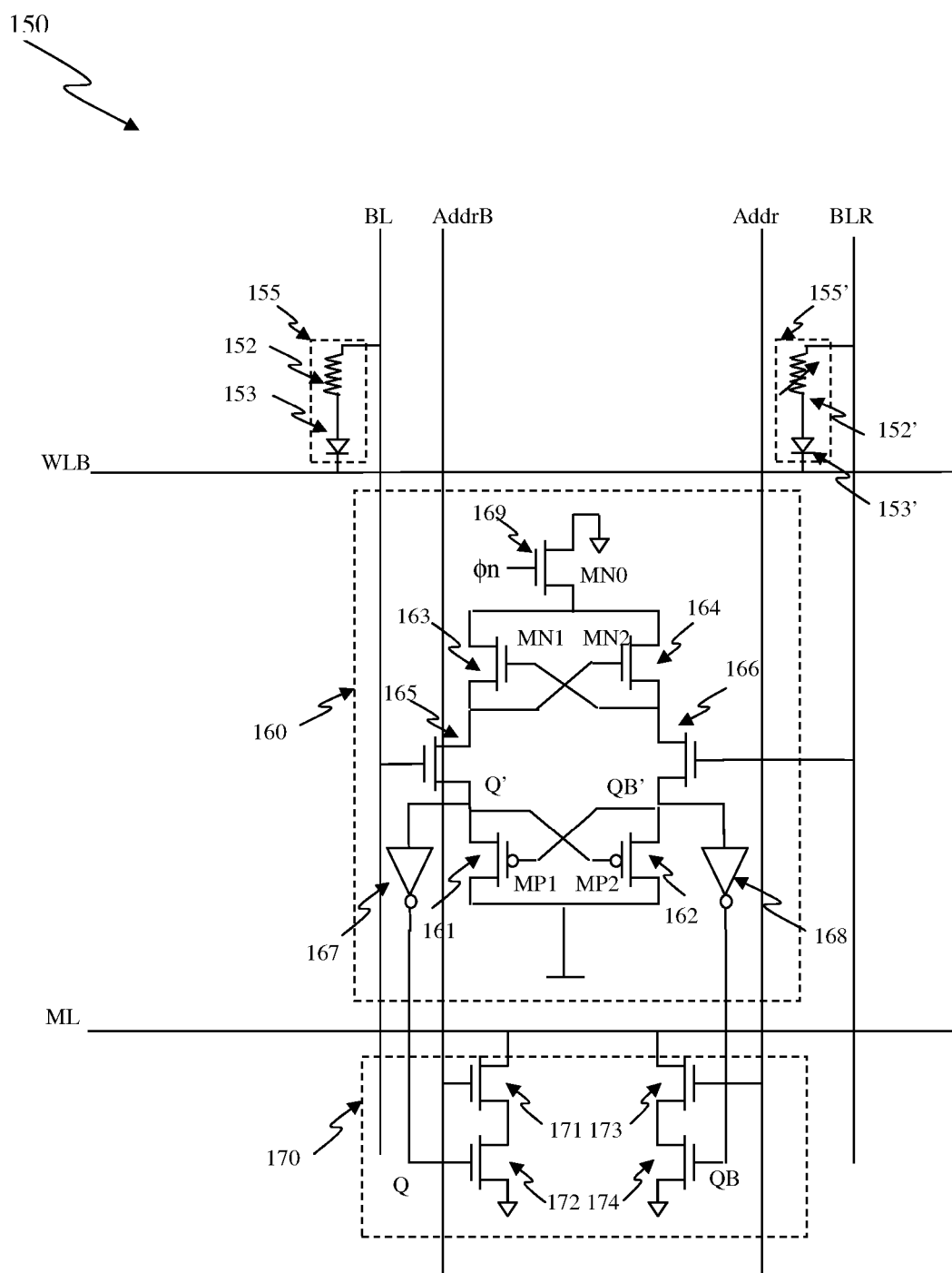


FIG. 3(c)

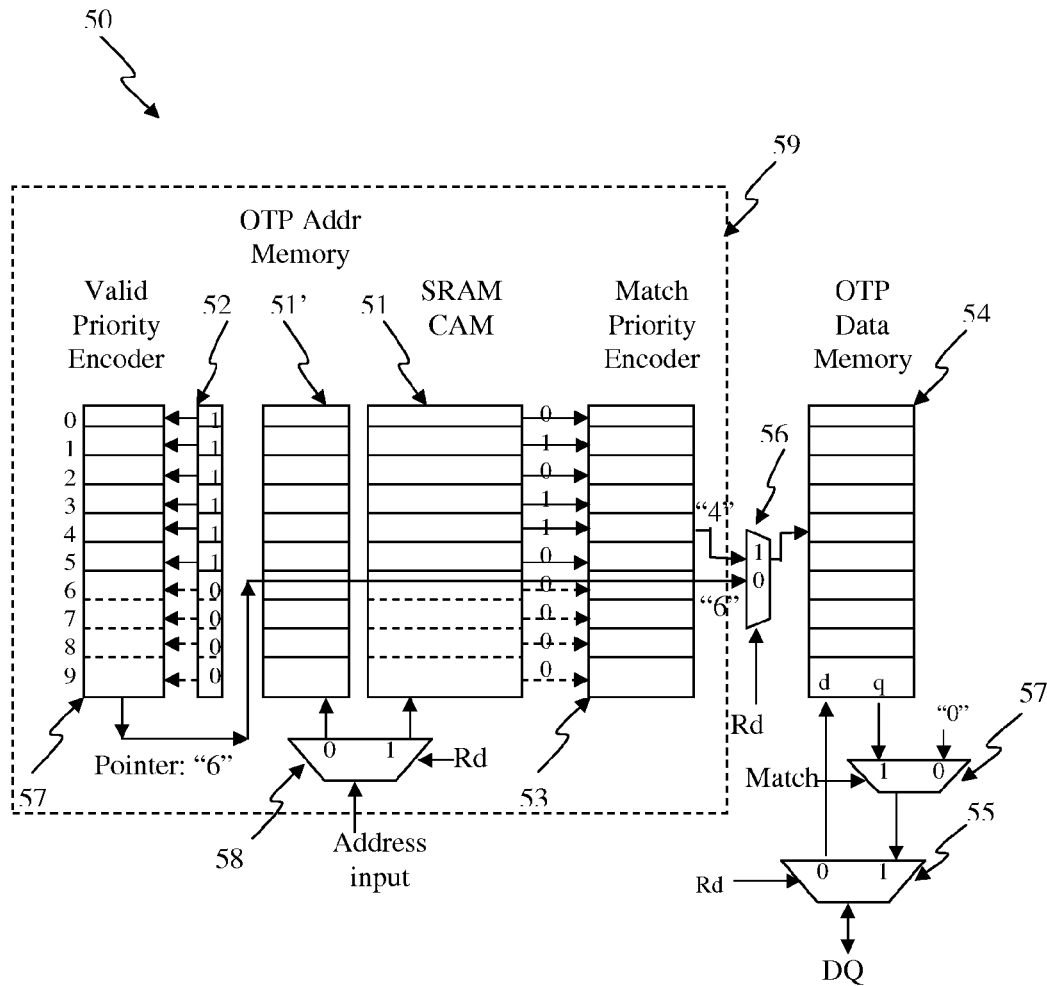


FIG. 4(a)

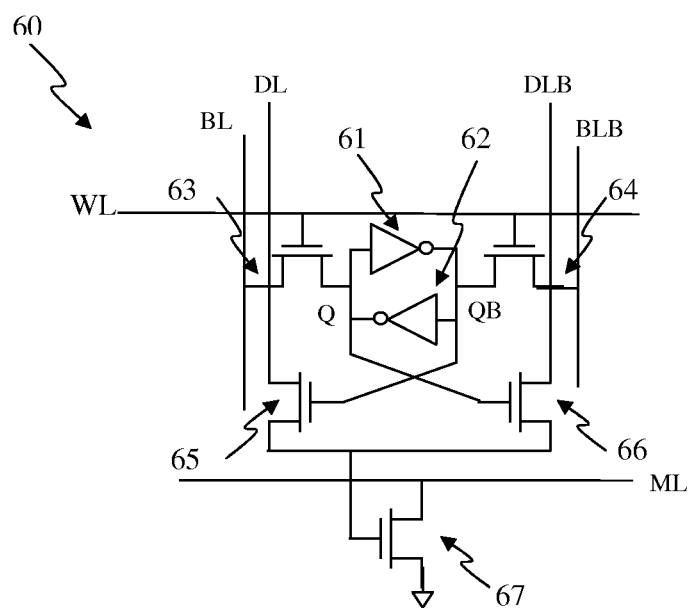
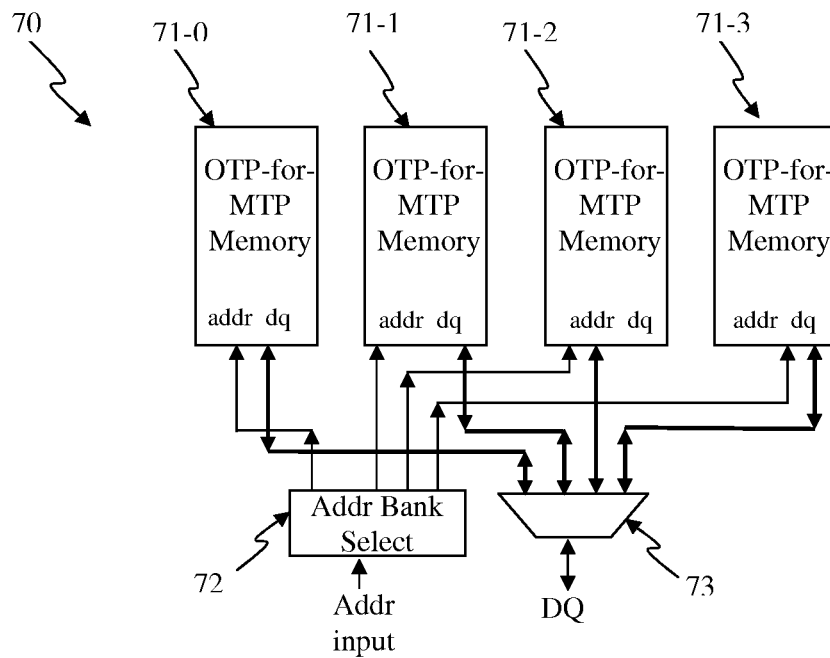
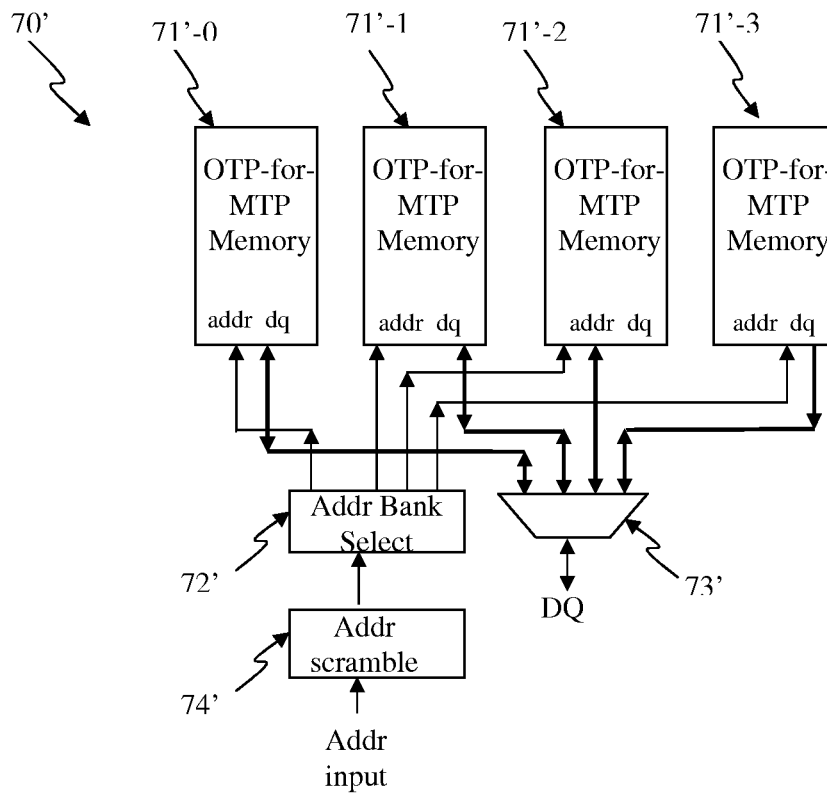


FIG. 4(b)

**FIG. 5(a)****FIG. 5(b)**

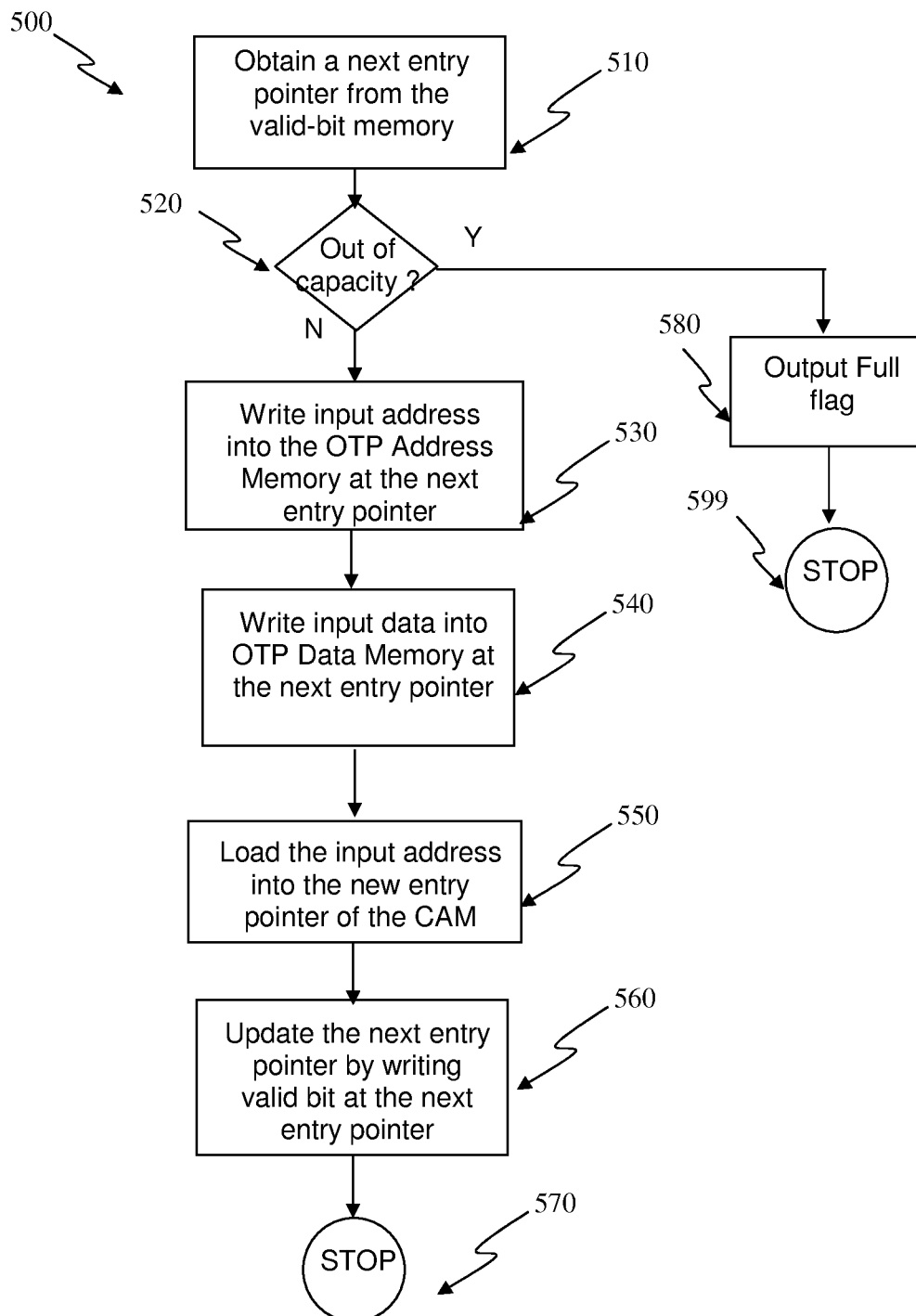


FIG. 6

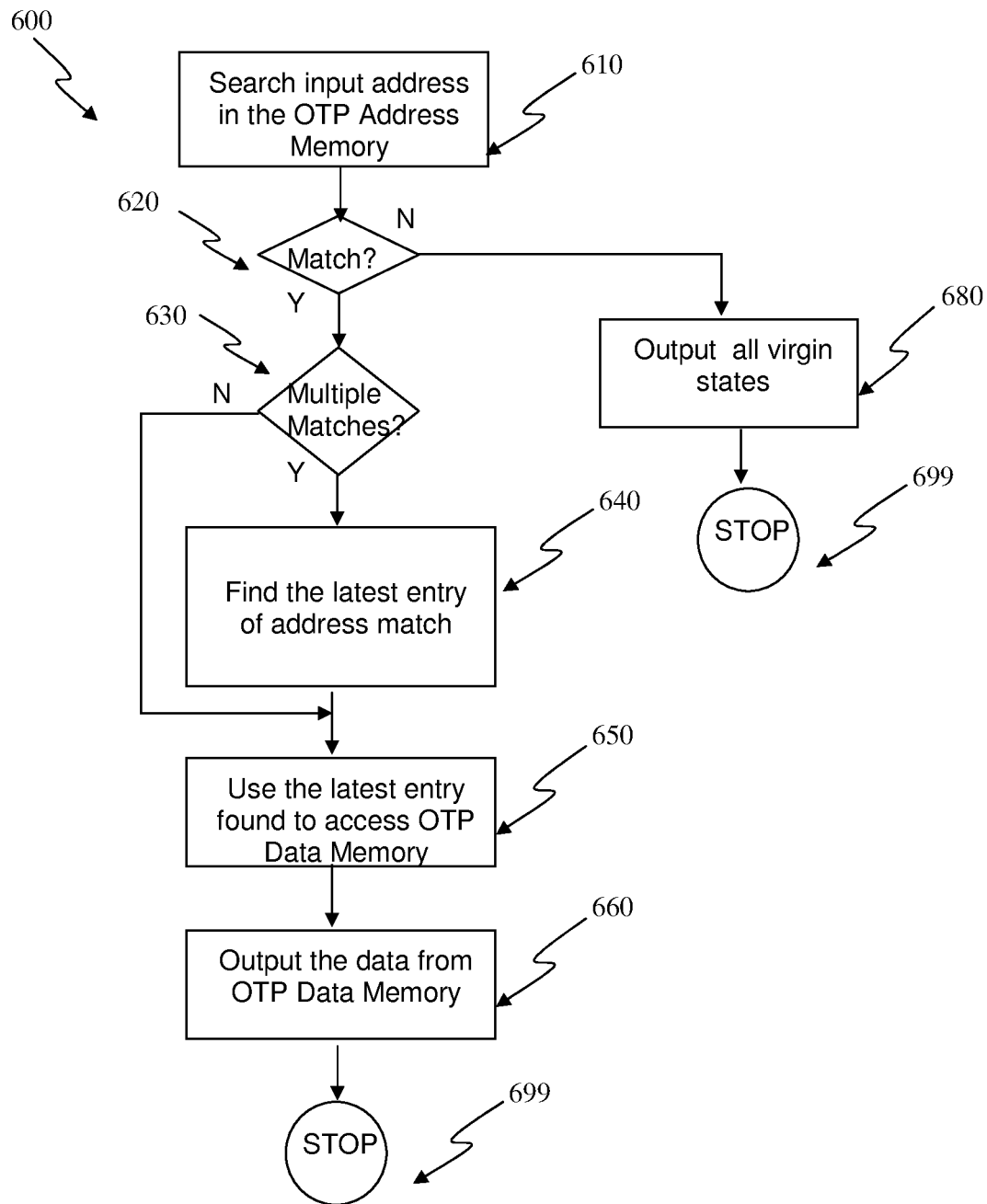


FIG. 7

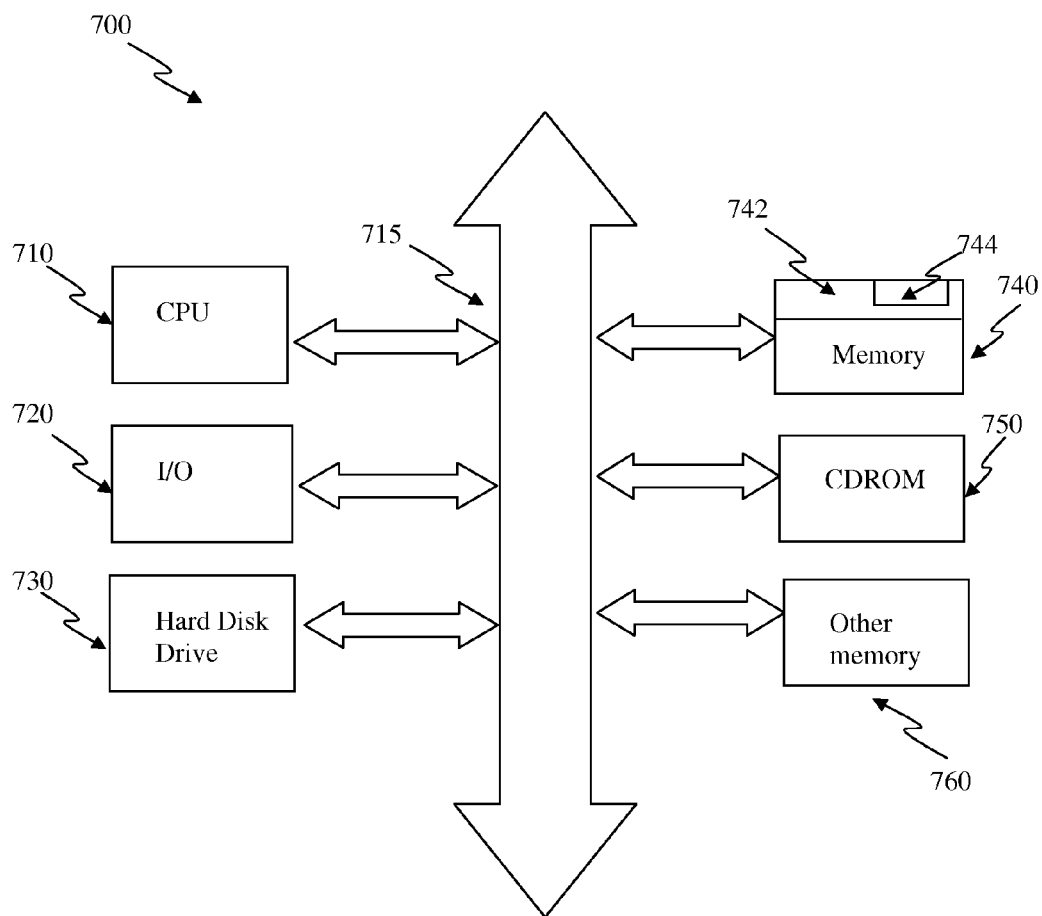


FIG. 8

OTP MEMORIES FUNCTIONING AS AN MTP MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority benefit of U.S. Provisional Patent Application No. 61/699,255, filed on Sep. 10, 2012 and entitled "System and Method of Using OTP Memories to Function as An MTP Memory," which is hereby incorporated herein by reference.

BACKGROUND

One Time Programmable (OTP) memory can be fabricated in standard logic processes but can only be programmed once. Multiple-Time Programmable (MTP) memory can be programmed many times but fabrication requires special process steps and masks.

FIG. 1 shows a block diagram of a portion of a conventional OTP-for-MTP memory 10. An OTP-for-MTP memory is a physical OTP memory but appears to be capable of being programmed into the same address multiple times without the need to first erase data. The OTP-for-MTP memory 10 has 5 OTP banks, 12-0 through 12-4, with addresses and data coupled to external address and data bus DQ, respectively, through a multiplexer 13. The multiplexer 13 receives a bank select signal to route the external address/DQ to the address/DQ of each OTP bank 12-0 through 12-4, depending if the programming is the 1st, 2nd, 3rd, 4th or 5th time. In general, an n-time programmable MTP memory can be realized by using n arrays of the same size OTP memory for each time programming.

The techniques of using OTP to function as MTP as showed in FIG. 1 is relatively simple, but are not very efficient or cost effective. First, the size of the conventional MTP increases proportionately to the number of times it can be programmed. For example, for a 100-time MTP, a base OTP memory needs to be replicated 100 times to achieve the same functionality. Second, data utilization by the convention MTP is not very efficient. If the data in only one address of an OTP-for-MTP memory is programmed 100 times while the rest of the data stays the same, 99% of the programmability of the entire OTP memory capacity is wasted. Therefore, there is a need for improved techniques to achieve low cost, high data utilization, and efficient OTP-for-MTP memories.

SUMMARY

Techniques, systems and circuitry for using One-Time Programmable (OTP) memories to function as a Multiple-Time Programmable (MTP) memory are disclosed. The OTP-for-MTP memory can include at least one OTP data memory to store data, and at least one OTP CAM to store addresses and to search input address through valid entries of the OTP CAM to find a latest entry of the matched valid addresses. The OTP-for-MTP memory can also include a valid-bit memory to find a next available entry of the OTP data memory and OTP CAM. When programming data into the OTP-for-MTP memory, the address and data can be both programmed into the next available entry of the OTP CAM and the OTP data memory, respectively. When reading the OTP-for-MTP memory, the input address can be used to compare with valid entries of the addresses stored in the OTP CAM so that the latest entry of the matched valid addresses can be output. The latest entry can then be used to access the OTP data memory to retrieve data for output.

Embodiments disclosed herein use various schemes to make OTP memories to function as an MTP memory effectively. In one embodiment, the OTP-for-MTP memory can include at least one OTP address memory, at least one OTP data memory, and at least one OTP valid-bit memory. The three types of OTP memories can all have a plurality of entries and they are all associated with each other for each entry. When programming the OTP-for-MTP memory, the address and data can be both programmed into a new entry of OTP address memory and OTP data memory, respectively. The valid bit in the same entry of the OTP valid memory can also be programmed and a new entry can be updated. The new entry can be to be updated in a predetermined way, or simply in the increment/decrement order. Data at the same address can be programmed into the OTP-for-MTP repetitively in the new entries of the OTP address and data memory, until reaching the capacity limit of the OTP address and data memory. When reading data from the OTP-for-MTP, the input address can be searched through the entire valid OTP address memory. If there are any matches, the data in the OTP data memory associated with the latest entry of the valid matched address can be accessed for output; otherwise all bits with virgin state (normally "0") would be used for output. By using this approach, any data for any address can be programmed into the OTP-for-MTP many times without any restrictions or fixed compartments until the total capacity of the OTP address/data memory is reached.

The invention can be implemented in numerous ways, including as a method, system, device, or apparatus (including graphical user interface and computer readable medium). Several embodiments of the invention are discussed below.

As a memory, one embodiment can, for example, include at least one OTP address memory; at least one OTP data memory, at least one OTP valid-bit memory, a new entry generation block, at least one match block, and one multiple-match select block. Each type of the OTP memory has at least one entry and each entry can be associated with each other. When programming data into the OTP-for-MTP memory, the data and address can both be programmed into a new entry of OTP data and address memory, respectively. Valid bit in the new entry of the OTP valid memory can also be programmed, and a new entry is updated in the new entry generation block according to a predetermined order. When reading data from an address in the OTP-for-MTP, the address is searched through all valid entries of the OTP address memory by the match block. If there are any matches found, the latest entry of the valid matched address can be provided by the multiple-match select block based on new entry update order. The latest entry of the valid matched addresses can be used to access the OTP data memory for output. If no matches are found, a word with all virgin state (i.e. "0") can be used for output instead.

As a non-volatile memory, one embodiment can, for example, include at least: at least one One-Time Programmable (OTP) data memory that has a plurality of OTP memory cells to store data; and at least one OTP Content Addressable Memory (CAM) that has a plurality of OTP address memory cells to store valid addresses and a plurality of CAM memory cells to compare an input address with the valid addresses stored in the OTP address memory cells and to output a latest entry of the matched valid addresses. The non-volatile memory can be configured to be programmable multiple times on the same addresses by programming an address and data into a next available entry of the OTP CAM and the OTP data memory, respectively. The non-volatile memory can be configured to be read by using the input address to search the latest entry of the matched valid

addresses in the OTP CAM and then use that address to access the OTP data memory to read data for output.

As an electronic system, one embodiment can, for example, include at least: a processor; and at least an OTP-for-MTP memory operatively connected to the processor. The OTP-for-MTP memory can include at least: an OTP address memory, an OTP data memory, an OTP valid-entry memory, a new entry generation, a match block, and a multiple-match select block. The OTP address memory, OTP data memory, and the OTP valid-entry memory all have at least one entry and each entry is associated with each other. When the processor programs the OTP-for-MTP, the address and data can both be programmed into a new entry of OTP address and OTP data memories, respectively. A valid bit can also be programmed in the new entry of the OTP valid memory. A new entry can be updated subsequently determined by the new entry generation block. The process of programming can continue until reaching the total capacity of the OTP address memory or OTP data memory. When the processor reads data through all valid entries of the OTP address memory by the match block. If there are any matches found, the latest entry of the valid matched addresses can be determined by the multiple-match select block according to the entry update order. Subsequently, the data in the latest entry of the valid matched address in the OTP data memory can be accessed as output. If no matches are found, a word with all virgin state (e.g. "0") will be sent as output.

As an electronic system, one embodiment can, for example, include at least: a processor and an MTP memory based on OTP memory operatively connected to the processor. The MTP memory can include: an OTP data memory having a plurality of entries of OTP memory cells to provide data storage; an OTP Content Addressable Memory (CAM) having a plurality of entries of OTP memory cells and CAM cells to provide address storage and to search an input address among valid addresses stored in the OTP memory cells and to output a latest entry of the matched valid address; and at least one register to provide a next available entry in the OTP data memory and OTP CAM. The MTP memory is configured to be programmable by programming an address and data into the next available entry in the OTP CAM and the OTP data memory, respectively. The MTP memory is configured to be read by searching an input address in the OTP CAM and providing the latest entry of the matched valid address to access the OTP data memory to read data for output.

As a method for making OTP memories to function as an MTP memory, one embodiment can, for example, include at least: providing at least one OTP address memory, at least one OTP data memory, at least one OTP valid-entry memory, a new entry generation method, a search method and a multiple-match resolution method. The OTP address memory, OTP data memory, and OTP valid entry memory have at least one entry. Each entry in the three types of OTP memories is associated with each other. The method to program an OTP-for-MTP memory can include (i) finding a new entry in the OTP address and data memories, (ii) programming the address and data into a new entry of the OTP address and OTP data memories, respectively; (iii) programming a valid bit associated with the new entry in the OTP valid memory; (iv) updating a new entry based on a pre-determined order. The method to read an OTP-for-MTP memory includes (i) searching the input address through the entire valid entries in the OTP address memory to find any entries of valid matched address, (iii) finding the latest entry if multiple matches occur, (ii) outputting data in the OTP data memory associated with

the latest entry in the match addresses; and (iii) outputting data with all bits in virgin state, if no matches are found.

As a method of providing an MTP memory based on OTP memories, one embodiment can, for example, include at least: providing at least an OTP memory having a plurality of entries of OTP memory cells to store data; providing at least an OTP CAM having a plurality of entries of OTP memory cells to store valid addresses and a plurality of entries of CAM memory cells to compare an input address with valid addresses stored and outputting a latest entry of the matched valid addresses; finding the next available entry of the OTP data memory and OTP CAM; programming data and address into the next available entry of the OTP data and OTP CAM, respectively, when programming the MTP memory; and searching input address in all valid addresses stored in the OTP CAM to find the latest entry of the matched valid addresses to access the OTP data memory when reading the MTP memory.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed descriptions in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIG. 1 shows a block diagram of a conventional OTP-for-MTP memory.

FIG. 2(a) shows a block diagram of an OTP-for-MTP in a program operation according to one embodiment.

FIG. 2(b) shows a block diagram of an OTP-for-MTP in a read operation according to one embodiment.

FIG. 2(c) shows a diagram of a portion of an OTP-for-MTP memory according to one embodiment.

FIG. 3(a) shows a block diagram of a portion of an OTP-for-MTP memory according to one embodiment.

FIG. 3(b) shows a logic block diagram of a portion of a row in the OTP Content-Addressable Memory (CAM) according to one embodiment.

FIG. 3(c) shows a circuit block diagram of a portion of a cell in one OTP CAM according to one embodiment.

FIG. 4(a) shows a block diagram of a portion of an OTP-for-MTP memory functional block according to another embodiment.

FIG. 4(b) shows a circuit diagram of a CAM cell in the SRAM CAM memory of FIG. 4(a) according to one embodiment.

FIG. 5(a) shows a block diagram of a portion of multiple segment OTP-for-MTP memory according to one embodiment.

FIG. 5(b) shows a block diagram of a portion of multiple segment OTP-for-MTP memory with address scramble block according to another embodiment.

FIG. 6 depicts a method in a flow chart to program an OTP-for-MTP memory according to one embodiment.

FIG. 7 depicts a method in a flow chart to read an OTP-for-MTP memory according to one embodiment.

FIG. 8 shows an electronic system using at least one OTP-for-MTP memory.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Embodiments disclosed herein use various techniques to use OTP memories to emulate the functionality of an MTP memory. An OTP-for-MTP memory can appear to be programmable into the same addresses of an OTP memory multiple times (e.g., without being erased first).

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Techniques, systems and circuitry for using One-Time Programmable (OTP) memories to function as a Multiple-Time Programmable (MTP) memory are disclosed. The OTP-for-MTP memory can include at least one OTP data memory to store data, and at least one OTP CAM to store addresses and to search input address through valid entries of the OTP CAM to find a latest entry of the matched valid addresses. The OTP-for-MTP memory can also include a valid-bit memory to find a next available entry of the OTP data memory and OTP CAM. When programming data into the OTP-for-MTP memory, the address and data can be both programmed into the next available entry of the OTP CAM and the OTP data memory, respectively. When reading the OTP-for-MTP memory, the input address can be used to compare with valid entries of the addresses stored in the OTP CAM so that the latest entry of the matched valid addresses can be output. The latest entry can then be used to access the OTP data memory to retrieve data for output.

In one embodiment, data and address can be recorded in OTP memories in a certain order whenever a programming occurs. During read, data associated with the latest address that has been programmed can be read from the OTP memory.

Several embodiments of the invention are discussed below with reference to FIGS. 2(a)-8. However, those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes as the invention extends beyond these limited embodiments.

FIG. 2(a) shows a block diagram to indicate a program operation in an OTP-for-MTP memory 100 according to one embodiment. The OTP-for-MTP memory 100 has an OTP address CAM (Content Addressable Memory) 101 to store the addresses and an OTP data memory 102 to store the input data during programming. The OTP address CAM 101 has a pointer to indicate the next available entry for programming. When programming into the OTP-for-MTP memory 100, the input address and data are programmed into the address CAM 101 and the OTP data memory 102, respectively. The next entry pointer is updated subsequently.

FIG. 2(b) shows a block diagram to indicate a read operation in an OTP-for-MTP memory 100' according to one embodiment. The OTP-for-MTP memory 100' has an OTP address CAM (Content Addressable Memory) 101' to store the addresses and an OTP data memory 102' to store the associated data. The OTP address CAM 101' has a new entry pointer to differentiate between filled and empty entries. When reading the OTP-for-MTP memory 100', the input address is used to search among the filled entries in the OTP Address CAM 101' that match the input address, and to find the latest match if there are multiple matches. The latest match address is used to access the OTP Data Memory 102' for an output DQ. If no match is found, a word of all virgin state will be output to DQ.

FIG. 2(c) illustrates a diagram of a portion of an OTP-for-MTP memory 20 according to one embodiment. The OTP-for-MTP memory 20 has an OTP Address CAM 29, an OTP Data Memory 24, and several address, data, or I/O multiplexers 26, 27 and 25. The OTP Address CAM 29 can include an OTP Address Memory 21, a match block 22, and a multiple match select block 23 to store the input addresses, to match the input address in the OTP Address Memory 21, and to resolve multiple matches if any, respectively. The match block 22 is coupled to the OTP Address Memory 21 to find any address matched, and is coupled to the multiple match select block 23 to resolve any multiple matches. The OTP Data Memory 24 is to store the actual data that is programmed and read. The address multiplexer 26 is to multiplex between

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input address and the latest match address for programming and reading, respectively, as an address to the OTP Data Memory 24. The multiplex 25 is an I/O multiplexer to multiplex between input or output data for program or read, respectively. The multiplexer 27 is a match/non-match multiplexer to output the data in the OTP Data Memory if match or a word of all virgin state if non-match happens.

When programming the OTP-for-MTP memory 20, both the address and data are programmed into a new entry of the OTP address memory 21 and the OTP data memory 24, respectively. The next new entry pointer is updated in a predetermined order. When reading the OTP-for-MTP memory 20, the input address is checked against all addresses stored in the OTP address memory 21 by the match block 22. The match block 22 sends all entries of the valid matched addresses to the multiple-match select block 23 to find the latest entry. Then, the latest entry is used as an address to access data in the OTP data memory 24 that is to be output. If no matches are found, all bits with a virgin state will be output through the output multiplexer 25.

FIG. 3(a) shows a block diagram of a portion of an OTP-for-MTP memory 30 according to one embodiment. The OTP-for-MTP memory 30 has an OTP Address CAM 39, an OTP Data Memory 34, and address, data, or I/O multiplexers 36, 37 and 35, respectively. The OTP Content Addressable Memory 39 can include an OTP CAM Array 31, a valid-bit memory 32, a Next Entry Encoder 37, and a Match Priority Encoder 33. The OTP CAM Array 31 has a plurality of entries that can be programmed only once and can be used to search the stored contents with the input address and to output entry numbers, if any, that match. The OTP valid-bit memory 32 has a plurality of entries that can be programmed only once to indicate the validity of the entries. For example, the entries 0 through 5 in FIG. 3(a) are marked as "1" as being programmed, which means these entries in the OTP CAM Array 31 and OTP Data Memory 34 contain valid information. The Next Entry Encoder 37 can be used to determine the next new entry number, i.e. "6", based on valid bits. The easiest way to determine the next new entry is to search through the entry number increasingly or decreasingly until the first un-programmed valid bit is found. For example, the next available entry can be "6," since the entries 0 through 5 have been used. This can be achieved by using a priority encoder (or leading 1/0 detector) to detect the location of a first "1/0" after searching a long string of "0s" or "1s." The Match Priority Encoder 33 accepts all match addresses from the OTP CAM Array 31 to determine the latest entry of the match addresses, for example, the highest entry number of the match address. The Match Priority Encoder 33 can be embodied as another priority encoder based on the match line outputs from the OTP CAM Array 31, such as finding the first "1" from left to right in the string "0101100000" of match lines as shown in FIG. 3(a). The first "1" is found at entry "4." The latest entry number (i.e., 4) can be used as an address to access the OTP Data Memory 34 through a read/write multiplexer 36. The data accessed from the OTP Data Memory 34 can be used as an output DQ through the I/O multiplexer 35 (or output multiplexer) if any match occurs; otherwise all bits in virgin state will be outputted through the data multiplex 37.

FIG. 3(b) shows a block diagram of a portion of a row 40 in an OTP CAM Array in FIG. 3(a) according to one embodiment. The row 40 is a logic implementation of a row in the OTP CAM Array 31 in FIG. 3(a). A row of the OTP CAM Array 40 has w cells 41-0 through 41-(w-1) for a w-bit word to store addresses. Each cell 41-i (i=0, 1, 2, . . . , w-1) has an OTP unit that contains an OTP data cell 42, an OTP reference cell 43, a sense amplifier 44, and a CAM unit 49 that contains

a latch **45** and an XNOR **46**. The XNOR **46** compares the data stored in the latch **45** with the incoming address bit to output a MAT: "1" if the data are the same or "0" if not. The MAT of each cell in the same row is AND'd to output a match line ML-j, for the jth row.

FIG. 3(c) shows a block diagram of a portion of an OTP CAM cell **150** according to one embodiment. The cell **150** in FIG. 3(c) is a circuit implementation of the cell **40-i** in FIG. 3(b). An OTP data cell **155**, corresponding to the OTP data cell **42** in FIG. 3(b), that has an OTP element **152** coupled to a diode **153** as a selector. One end of the OTP element **152** is coupled to a bitline (BL) and the other end coupled to a wordline bar (WLB). An OTP reference cell **155'**, corresponding to the OTP reference cell **43** in FIG. 3(b), that has an OTP reference element **152'** coupled to a diode **153'** as a selector. One end of the reference OTP element **152'** is coupled to a reference bitline (BLR) and the other end coupled to the same wordline bar (WLB). A sense amplifier **160** that corresponds to the sense amplifier **44** in FIG. 3(b). The sense amplifier **160** has a pair of PMOS **161** and **162** with their gates and drains cross-coupled and their sources coupled to a supply voltage. The drains of the PMOS Q' and QB' are coupled to the drains of NMOS **165** and **166**, respectively. The gates of the NMOS **165** and **166** are coupled to BL and BLR, respectively. The sources of the NMOS **165** and **166** are coupled to the drains of the NMOS **163** and **164**, respectively. The gate of NMOS **163** is coupled to the drain of the NMOS **164**, and the gate of NMOS **164** is coupled to the drain of NMOS **163**. The sources of the NMOS **163** and **164** are coupled to the drain of an NMOS **169**. The gate of the NMOS **169** is coupled to a sensing control signal ϕ_n the source is coupled to the ground. The drains of the PMOS **161** and **162** are coupled to the inputs of two inverters **167** and **168**, respectively. The outputs of the inverters **167** and **168** Q and QB are the output of the sense amplifier **160**. An exclusive NOR (XNOR) **170**, part of a wired OR'd match line (ML) in the cell **150**, that has two pairs of NMOS devices in serial with their gates coupled to Q and AddrB in one pair and QB and Addr in the other pair. The two pairs of NMOS in serial have one end coupled to ground and the other ends coupled to a match line (ML) common to all cells in the same row.

The OTP data cell **42** or the reference cells **43** in FIG. 3(b) are all OTP cells that can have an OTP element coupled to at least one program selector. The OTP element can be an electrical fuse or anti-fuse, depending if the programmed state has higher or lower resistance than that of the virgin state. The program selector can be a MOS or diode. The electrical fuse element can be an interconnect that consists at least a portion of the polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, thermally isolated active region, metal, metal alloy, MOS gate, or combination thereof. The electrical fuse element can also be a single or a plural of contact or via. The anti-fuse can be a dielectric breakdown anti-fuse with a thin layer of dielectric between electrodes or in a contact/via hole. Alternatively, the anti-fuse can be a gate-oxide breakdown anti-fuse by breaking down the thin oxide in a MOS gate. The OTP reference cell is more desirable to be built with the same material or structure as the OTP data cell for better device matches during sensing. The sense amplifier **160** is a latch-type of sense amplifier that can sense a small differential signal developed between BL and BLR by asserting the signal ϕ_n when the BL and BLR pull-up devices (not shown in FIG. 3(c)) are turned on. **170** is a pass-gate implementation of XNOR between the output Q/QB of the sense amplifier **160** and the Addr/AddrB input. The output ML of the XNOR **170** is coupled to the same ML for those cells in the same row.

There are many varieties and equivalent embodiments of OTP data/reference cells, sense amplifier, or XNOR circuit in FIG. 3(c). For example, the OTP cell can have a MOS as selector, though a diode is a more desirable embodiment. The input MOS devices **165** and **166** of the sense amplifier **160** can be placed near the supply voltage or ground instead of placed between N-latch and P-latch as shown in FIG. 3(c). The pair of the inverter **167** and **168** may be omitted in other embodiments. There can be many different latch types of sense amplifiers. The XNOR circuit **170** can be embodied in combinational logic, instead of a domino logic as shown in FIG. 3(c). The MOS in FIG. 3(c) can be either NMOS or PMOS. For those skilled in the art understand that the above descriptions are for illustrative purposes and there are many various and equivalent embodiments that are still within the scope of this invention.

FIG. 4(a) shows a block diagram of a portion of an OTP-for-MTP memory **50** according to one embodiment. The OTP-for-MTP memory **50** has at least one OTP Address CAM **59**, an OTP Data Memory **54**, and several address, data, and I/O multiplexers **56**, **57** and **55**, respectively. The OTP Address CAM **59** has at least an OTP Address Memory **51'**, at least one SRAM CAM **51**, at least one OTP valid-bit memory **52**, a Valid Priority Encoder **57**, and a Match Priority Encoder **53**. The OTP Address Memory **51'**, the SRAM CAM **51**, the OTP Data Memory **54**, and the OTP valid-bit memory **52** all have a plurality of entries to store non-volatile addresses, volatile addresses for comparison, data, and valid bits, respectively. The SRAM CAM **51** can be loaded with the addresses from the OTP address memory **51'**, which can be used to compare with any input address and output the latest entry number, if any, that matches. Both the OTP address memory **51'** and the SRAM CAM **51** can be updated during programming. But only the SRAM CAM **51** can be used for comparing with the input address during reading. The OTP valid-bit memory **52** stores valid bits to indicate the validity of each entry. For example, the entries 0 through 5 in FIG. 4(a) are marked as "1", programmed state, which means these entries in the Match Address Memory **51'** and OTP Data Memory **54** contain valid information. A valid Priority Encoder **53** can be used to determine the next new entry number, i.e. "6." The easiest way to determine the next new entry is to search in increasing or decreasing order through all the entries. For example, the next available entry can be "6," since the entries 0 through 5 have been used. This can be achieved by using a priority encoder, or leading 1/0 detector, to detect the location of a first "1/0" after searching a long string of "0s" or "1s." The Match Priority Encoder **53** can accept all match addresses from the SRAM CAM **51** to determine the latest entry of the match addresses, i.e. the match address stored in the highest entry if the next new entry is incremented. The Match Priority Encoder **53** can be embodied as another priority encoder based on the match line outputs, such as "0101100000" from entries 0 to 9. In FIG. 4(a), the match outputs are searched from entry 9 through 0 until the first "1" is found at entry "4." The latest entry number (i.e., 4) can be used as an address to access the OTP Data Memory **54** through a read/write address multiplexer **56**. The data accessed from the OTP Data Memory **54** can be used as an output DQ through an I/O multiplexer **55** if any match occurs; otherwise, all bits in the virgin state will be outputted through the data multiplex **57**.

FIG. 4(b) shows a circuit diagram of a SRAM CAM cell **60** corresponding to the memory cells of the SRAM CAM **51** in FIG. 4(a), according to one embodiment. The SRAM CAM cell **60** has an SRAM core that consists of a pair of cross-coupled inverters **61** and **62** and a pair of NMOS pass gates **63**

and 64. The two nodes Q and QB of the cross-coupled inverters 61 and 62 are coupled to the sources of NMOS 63 and 64, respectively. The gates of the NMOS 63 and 64 are coupled to a wordline (WL). The drains of NMOS 63 and 64 are coupled to BL and BLB, respectively. The sources/gates of NMOS 65 and 66 are coupled to DL/QB and DLB/Q, respectively. The drains of the NMOS 65 and 66 are coupled to the gate of NMOS 67, whose source is coupled to ground and drain is coupled to a match line (ML).

A priority encoder is to detect the location of a first 0 or 1 in a string of binaries. For example, a string as shown in the following:

bit	bit	bit	bit	bit	bit	bit	bit	bit	bit	bit	bit
0	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	1	0	1	1	1	0	1	1

A priority encoder to find the first 1 from bit 0 to bit 11 will output a "4" in decimal, or "100" in binary. There are many embodiments available for priority encoders. See, e.g., U.S. Pat. No. 5,383,142 for additional information on detecting bit patterns, which is hereby incorporated as a reference.

The OTP valid-bit memory 32 in FIG. 3(a) or the OTP valid-bit memory 52 in FIG. 4(a) can have an additional disable bit per entry. When a disable bit is programmed, the information in same entry in the OTP CAM unit and the OTP Data Memory will not be used, no matter whether the valid bit is programmed or not. The disable bit can be programmed any time while the OTP-for-MTP memory is active or when the chip is enabled or powering up. This provides a mechanism to simplify multiple match resolution and/or to abandon an entry if any bits in the OTP CAM unit or OTP data memory are defective.

FIG. 5(a) shows a block diagram of a portion of multiple segment OTP-for-MTP memory 70 according to one embodiment. The multiple segment OTP-for-MTP 70 has a plurality of OTP-for-MTP memories 71-0 through 71-3, corresponding to the OTP-for-MTP memory 30 in FIG. 3(a) or the OTP-for-MTP memory 50 in FIG. 4(a), with each OTP-for-MTP memory responsible for certain address ranges. For example, if the OTP-for-MTP memory 70 has 1 Kb of address, the OTP-for-MTP memories 71-0, 71-1, 71-2 and 71-3 are responsible for addresses 0-255, 256-511, 512-767 and 768-1023, respectively. Any address input to the OTP-for-MTP memory 70 will be routed into the proper OTP-for-MTP memory 71-0 through 71-3 based on the address ranges by an address bank select block 72. Similarly, the data input/output DQ can be routed to the DQ of the suitable OTP-for-MTP memory 71-0 through 71-3 by a multiplexer 73.

In another embodiment, addresses to each OTP-for-MTP can be assigned based on the address modulus to the number of banks. For example, OTP-for-MTP memories 71-0, 71-1, 71-2 and 71-3 can be assigned for those addresses that are 4 m+0, 4 m+1, 4 m+2, and 4 m+3, respectively, where m=0, 1, 2, 3, 4 This embodiment can divide the OTP-for-MTP memory into several smaller memories so that the speed can be faster and the overhead can be lower.

FIG. 5(b) shows a block diagram of a portion of multiple segment OTP-for-MTP memory 70' according to one embodiment. This embodiment is similar to that in FIG. 5(a) except an additional address scramble block 74' is included to spread the input address among different segments of OTP-for-MTP memories. The multiple segment OTP-for-MTP 70' has an input address scramble unit 74' and a plurality of OTP-for-MTP memory 71'-0 through 71'-3, corresponding to

the OTP-for-MTP memory 30 in FIG. 3(a) or the OTP-for-MTP memory 50 in FIG. 4(a), with each OTP-for-MTP memory responsible for certain address ranges. For example, if the OTP-for-MTP memory 70' has 1 Kb of address, the OTP-for-MTP memories 71'-0, 71'-1, 71'-2 and 71'-3 are responsible for address ranges 0-255, 256-511, 512-767 and 768-1023, respectively. Any address input to the OTP-for-MTP memory 70' will be routed into the proper OTP-for-MTP memories 71'-0 through 71'-3 based on the address ranges by an address bank select block 72'. Similarly, the data input/output DQ can be routed to the DQ of the suitable OTP-for-MTP memory 71'-0 through 71'-3 by a multiplexer 73'.

In another embodiment, addresses to each OTP-for-MTP can be assigned based on the address modulus to the number of banks. For example, OTP-for-MTP memories 71'-0, 71'-1, 71'-2 and 71'-3 can be assigned for those addresses that are 4 m+0, 4 m+1, 4 m+2, and 4 m+3, respectively, where m=0, 1, 2, 3, 4 This embodiment can divide the OTP-for-MTP memory into several smaller memories so that the speed can be faster and the overhead can be lower. The address scramble unit 74' can make each OTP-for-MTP memory's entries filled up more uniformly.

Those skilled in the art understand that the above discussions are for illustrative purposes and that there are many variations and equivalents in constructing OTP memory such as electrical fuse or anti-fuse, OTP CAM cell or SRAM CAM cell, priority encoder, sense amplifier, or exclusive NOR and that are all within the scope of this invention.

FIG. 6 shows a flow chart 500 depicting a method for programming data into an OTP-for-MTP memory as shown in FIGS. 2, 3(a)-3(c) and 4(a), according to one embodiment. The procedure starts at 510 to generate a next entry pointer by using valid bits in a OTP valid memory. Then, check if the next entry pointer is out of the memory capacity in step 520. If so, output an error signal in step 580 and stop in step 599. If not, write an input address at the next entry pointer of an OTP Address Memory in step 530. Next, write input data at the next entry pointer of an OTP Data Memory in step 540. The input address can then be loaded to the new entry pointer of a Content Addressable Memory (CAM). For example, the cells in the SRAM CAM 51 in FIG. 4(a) can also be updated at the new entry pointer in step 550 so that the CAM and the OTP Address Memory are synchronized. Further, a valid bit can be written at the next entry pointer of the OTP valid memory in step 560. This procedure stops in step 570 if no further data are to be written into the OTP-for-MTP memory.

FIG. 7 shows a flow chart 600 depicting a method for reading data in an OTP-for-MTP memory, according to one embodiment. The procedure starts at 610 to search if any addresses stored in the OTP address memory match an input address. At step 620, the procedure checks if a match is found. If there is no match, output all bits with the virgin state in step 680 and then stop in step 699. If there is a match in step 620, further check if there are multiple matches in step 630. If no multiple matches, go ahead to use the entry of the valid matched address to access an OTP data memory in step 650. If there are multiple matches, find the latest entry of the valid matched address by following the entry update order in step 640. In one embodiment, the latest entry can be the highest entry number of the valid matched addresses, if addresses and data are filled in increment order. The entry of the only valid matched address or the latest valid matched address can be used to access the OTP data memory in step 650. Then, output the data accessed from the OTP Data Memory in step 660 and stop in step 699.

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FIGS. 6 and 7 illustrate flow charts depicting embodiments of programming data into an OTP-for-MTP memory and reading data from an OTP-for-MTP memory, respectively, in accordance with certain embodiments. The methods 500 and 600 are described in the context of an OTP-for-MTP memory, such as the OTP-for-MTP memory 100, 100' and 20 in FIGS. 2(a), 2(b) and 2(c), respectively, the OTP-for-MTP memory 30 in FIG. 3(a), or the OTP-for-MTP memory 50 in FIG. 4(a). In addition, although described as a flow of steps, one of ordinary skill in the art will recognize that at least some of the steps may be performed in a different order, including simultaneously, or skipped.

FIG. 8 shows a processor system 700 according to one embodiment. The processor system 700 can include an OTP device 744, such as in an OTP cell array 742, in at least one OTP-for-MTP memory 740, according to one embodiment. The processor system 700 can, for example, pertain to an electronic system. The electronic system can include a Central Process Unit (CPU) 710, which communicate through a common bus 715 to various memory and peripheral devices such as I/O 720, hard disk drive 730, CDROM 750, OTP-for-MTP memory 740, and other memory 760. Other memory 760 is a conventional memory such as SRAM, DRAM, or flash, typically interfaces to CPU 710 through a memory controller. CPU 710 generally is a microprocessor, a digital signal processor, or other programmable digital logic devices. OTP-for-MTP memory 740 is preferably constructed as an OTP device 744. The OTP-for-MTP memory 740 typically interfaces to CPU 710 through a memory controller. If desired, the memory 740 may be combined with the processor, for example CPU 710, in a single integrated circuit.

The embodiments of invention can be implemented in a part or all of an integrated circuit in a Printed Circuit Board (PCB), or in a system (e.g., electronic system, computer system, memory system, etc.). The OTP device can be implemented as any electrical fuse or anti-fuse. An electrical fuse can be based on a segment of interconnect or a single or plural of contact/via. The anti-fuse can be based on breaking down a layer of dielectric between electrodes or in a contact/via hole, or breaking down a thin gate oxide of a MOS device.

Additional details on OTP devices can be found in: (i) U.S. patent application Ser. No. 13/214,183, filed on Aug. 20, 2011 and entitled "Method and System of Using One-Time Programmable Memory as Multi-Time Programmable in Code Memory of Processors," which is hereby incorporated herein by reference; (ii) U.S. patent application Ser. No. 13/471,704, filed on May 15, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference; (iii) U.S. patent application Ser. No. 13/026,752, filed on Feb. 14, 2011 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference; and (iv) U.S. patent application Ser. No. 13/026,656, filed on Feb. 14, 2011 and entitled "Circuit and System of Using Polysilicon Diode As Program Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference.

The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of certain embodiments of the present invention. Modifications and substitutions of specific process conditions and structures can be made without departing from the spirit and scope of the present invention.

The many features and advantages of the present invention are apparent from the written description and, thus, it is intended by the appended claims to cover all such features and advantages of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact

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construction and operation as illustrated and described. Hence, all suitable modifications and equivalents may be resorted to as falling within the scope of the invention.

What is claimed is:

1. A non-volatile memory, comprising:

at least one One-Time Programmable (OTP) data memory that has a plurality of OTP memory cells to store data; and

at least one OTP Content Addressable Memory (CAM) that has a plurality of OTP address memory cells to store valid addresses and a plurality of CAM memory cells to compare an input address with the valid addresses stored in the OTP address memory cells and to output a latest entry of the matched valid addresses,

wherein the non-volatile memory is configured to be programmable multiple times on the same addresses by programming an address and data into a next available entry of the OTP CAM and the OTP data memory, respectively, and

wherein the non-volatile memory is configured to be read by using the input address to search the latest entry of the matched valid addresses in the OTP CAM and then use that address to access the OTP data memory to read data for output.

2. A non-volatile memory as recited in claim 1, wherein the non-volatile memory comprises:

at least one register to indicate the next available entry in the OTP data memory and the OTP CAM.

3. A non-volatile memory as recited in claim 1, wherein the OTP CAM has a plurality of OTP CAM cells, and wherein at least one of the OTP CAM cells has at least one OTP memory cell coupled to at least one volatile CAM cell.

4. A non-volatile memory as recited in claim 1, wherein the OTP CAM has at least one OTP address memory array to store addresses coupled to at least one volatile CAM memory array for address match and output the latest entry of the matched valid addresses.

5. A non-volatile memory as recited in claim 1, wherein the OTP CAM unit has at least one OTP valid-bit memory to store at least one valid bit per entry, and wherein the valid bit in the same entry is also programmed when programming an entry of the OTP CAM unit and the OTP data memory.

6. A non-volatile memory as recited in claim 5, wherein the OTP CAM unit has at least one OTP disable bit for each entry of the OTP valid-bit memory.

7. A non-volatile memory as recited in claim 5, wherein the OTP CAM unit has a circuit to generate a next available entry for the OTP CAM based on the valid bits.

8. A non-volatile memory as recited in claim 1, wherein the OTP CAM unit has a plurality of match lines for each entry that can be asserted when the contents of the valid entry match the input address.

9. A non-volatile memory as recited in claim 8, wherein the OTP CAM unit has a match priority encoder to find the latest entry of the match addresses among the asserted match lines.

10. A non-volatile memory as recited in claim 1, wherein the non-volatile memory only processes a portion of a total address range, and wherein other non-volatile memories to processes other portions of the total address ranges, whereby the full address range is constructed for the non-volatile memory.

11. A non-volatile memory as recited in claim 1, wherein the OTP memory has a plurality of OTP memory cells, and wherein at least one of the OTP memory cell is an electrical fuse or anti-fuse.

12. A non-volatile memory as recited in claim 11, wherein the electrical fuse cell includes at least a portion of polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, metal, metal alloy, CMOS gate, or combination thereof.

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13. A non-volatile memory as recited in claim 1, wherein the OTP memory has a plurality of OTP memory cells, and wherein at least one of the OTP memory cell has at least one diode as program selector.

14. An electronic system, comprising:

a processor; and

an MTP memory based on OTP memory operatively connected to the processor, the MTP memory comprising:
an OTP data memory having a plurality of entries of OTP memory cells to provide data storage;

an OTP Content Addressable Memory (CAM) having a plurality of entries of OTP memory cells and CAM cells to provide address storage and to search an input address among valid addresses stored in the OTP memory cells and to output a latest entry of the matched valid address; and

at least one register to provide a next available entry in the OTP data memory and OTP CAM,

wherein the MTP memory is configured to be programmable by programming an address and data into the next available entry in the OTP CAM and the OTP data memory, respectively, and

wherein the MTP memory is configured to be read by searching an input address in the OTP CAM and providing the latest entry of the matched valid address to access the OTP data memory to read data for output.

15. An electronic system as recited in claim 14, wherein the OTP CAM has at least one OTP valid-bit memory to store at least one valid bit per entry, and wherein the valid bit of an entry is also programmed when programming the same entry in the OTP CAM and/or the OTP data memory.

16. An electronic system as recited in claim 15, wherein the OTP CAM has a circuit to generate a next available entry in the OTP CAM based on the valid bits.

17. A method of providing an MTP memory based on OTP memories, comprising:

providing at least an OTP memory having a plurality of entries of OTP memory cells to store data;

providing at least an OTP CAM having a plurality of entries of OTP memory cells to store valid addresses and

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a plurality of entries of CAM memory cells to compare an input address with valid addresses stored and outputting a latest entry of the matched valid addresses;
finding the next available entry of the OTP data memory and OTP CAM;

programming data and address into the next available entry of the OTP data and OTP CAM, respectively, when programming the MTP memory; and
searching input address in all valid addresses stored in the OTP CAM to find the latest entry of the matched valid addresses to access the OTP data memory when reading the MTP memory.

18. A method as recited in claim 17, wherein the OTP CAM has a plurality of entries of OTP CAM cells, and wherein at least one of the OTP CAM cells has at least one OTP memory cell coupled to at least one volatile CAM cell.

19. A method as recited in claim 17, wherein the OTP CAM has at least one OTP address memory array to store addresses and at least one volatile CAM memory array for address match and output the latest entry of the matched valid addresses.

20. A method as recited in claim 17, wherein the searching to find the latest entry of the matched valid addresses comprises:

(i) comparing the valid contents of the OTP CAM with the input address bit-by-bit for each entry;

(ii) asserting a match line for each valid entry if the content matches the input address; and

(iii) finding the latest entry among the asserted match lines.

21. A method as recited in claim 20, wherein the searching to find the next available entry in the OTP CAM and the OTP data memory comprises:

(i) providing at least one valid bit for each entry of the OTP CAM and the OTP data memory;

(ii) programming the valid bit in the same entry after programming an entry of the OTP CAM and OTP data memory; and

(iii) finding the next entry with the valid bit unprogrammed in the entry update order.

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